WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

first and second lines arranged with a first interval; and

third and fourth lines arranged with a second interval wider than the first internal; wherein

the first internal is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the third and fourth lines is greater than a maximum value of a voltage generated between the first and second lines.

2. The semiconductor device according to claim 1, wherein the second line is connected to a first contact plug having the width larger than that of the second line, and the distance between the first line and the first contact plug is narrower than the first interval.

3. The semiconductor device according to claim 2, wherein the fourth line is connected to a second contact plug having the width larger than that of the fourth line, and the distance between the third line and the second contact plug is narrower than the second interval.

4. The semiconductor device according to claim 1, wherein the first and second line and the third and fourth lines are formed on the same wiring layer.

5. The semiconductor device according to claim 1, wherein the first and second line and the third and

fourth lines are formed on a different wiring layer.

6. The semiconductor device according to claim 1, further comprising a memory cell array; wherein

the first and second lines are arranged within the memory cell array.

7. The semiconductor device according to claim 1, further comprising a memory cell array; wherein

the first and second lines are bit lines arranged within the memory cell array.

8. The semiconductor device according to claim 1, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

9. The semiconductor device according to claim 3, wherein when the distance between the first line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth lines is assumed to be V2, the distance between the third line and the second contact plug Sb is expressed by $Sb = (V2/V1) \times Sa$.

10. A semiconductor device comprising:

first and second lines in a wiring layer arranged

with a first interval;

a third line arranged in the wiring layer, wherein a second interval between the first and third lines is wider than the first interval; and

a first transistor configured to connect the second and third lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated between the first and second lines.

11. The semiconductor device according to claim 10, wherein the second line is connected to the first transistor through the wiring layer formed just under the second line, and the third line is connected to the first transistor through the wiring layer formed just under the third line.

12. The semiconductor device according to claim 10, further comprising a memory cell array; wherein

the first and second lines are arranged within the memory cell array.

13. The semiconductor device according to claim 10, further comprising a memory cell array; wherein

the first and second lines are bit lines arranged within the memory cell array.

14. The semiconductor device according to claim 13, wherein the third line is a line to give a predetermined potential to the second line, during read operation.

15. The semiconductor device according to claim 13, wherein the third line is a line to connect the second line to a sense amplifier.

16. The semiconductor device according to claim 13, wherein the transistor turns off, the first and second line has an erase potential and the third line has a power supply potential, during erase operation.

17. The semiconductor device according to claim 10, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the first and third lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

18. The semiconductor device according to claim 10, wherein the second line is connected to a first contact plug having the width larger than that of the second line, and the distance between the first line and the first contact plug is narrower than the first interval.

19. The semiconductor device according to claim 18, wherein the third line is connected to

a second contact plug having the width larger than that of the third line, and the distance between the first line and the second contact plug is narrower than the second interval.

20. The semiconductor device according to claim 19, wherein when the distance between the first line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the first and third lines is assumed to be V2, the distance between the first line and the second contact plug Sb is expressed by $Sb = (V2/V1) \times Sa$.

21. The semiconductor device according to claim 10, further comprising a second transistor connected to the first line; wherein

the first and second transistors are arranged in being adjacent in the extending direction of the first and second lines.

22. The semiconductor device according to claim 21, wherein the second transistor is connected to between the first and third lines.

23. A semiconductor device comprising:

first and second lines in a wiring layer arranged with a first interval;

a third line arranged in the wiring layer;

a first transistor configured to connect

the second and third lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated between the first and second lines, and the third line is arranged at a position not adjacent to the first line.

24. The semiconductor device according to claim 23, wherein the second line is connected to the first transistor through the wiring layer formed just under the second line, and the third line is connected to the first transistor through the wiring layer formed just under the third line.

25. The semiconductor device according to claim 23, further comprising a memory cell array; wherein

the first and second lines are arranged within the memory cell array.

26. The semiconductor device according to claim 23, further comprising a memory cell array; wherein

the first and second lines are bit lines arranged within the memory cell array.

27. The semiconductor device according to claim 26, wherein the third line is a line to give a predetermined potential to the second line, during read operation.

28. The semiconductor device according to claim 26, wherein the third line is a line to connect the second line to a sense amplifier.

29. The semiconductor device according to claim 26, wherein the transistor turns off, the first and second line has an erase potential and the third line has a power supply potential, during erase operation.

30. The semiconductor device according to claim 23, further comprising a fourth line arranged in being adjacent to at least one of the first, second and third lines; wherein

the fourth line is a dummy line set to be floated its potential.